ABSTRACT

Interconnection structures for integrated circuits have first cells disposed in a first plane, at least second cells disposed in at least a second plane parallel to the first plane, and vertical interconnections disposed for connecting conductors in the first plane with conductors in the second plane, at least some of the vertical interconnections initially incorporating antifuses. The antifuses may be disposed over conductors that are disposed on a base substrate. The antifuses are selectively fused to prepare the integrated circuit for normal operation. Methods for fabricating and using such vertical interconnection structures are disclosed.